WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a plurality of leads, each of the leads defining first and second surfaces;

a semiconductor chip defining opposed first and second surfaces and including a plurality of input/output pads disposed on the first surface thereof;

a plurality of conductive bumps electrically connecting the input/output pads to the second surface of a respective one of the leads; and

an encapsulant portion covering the semiconductor chip, the conductive bumps, and the second surfaces of the leads such that at least portions of the first surfaces of the leads are exposed within the encapsulant portion.

2. The semiconductor package of Claim 1 wherein the first surface of the semiconductor chip is disposed at a prescribed separation distance from the second surfaces of the leads.

3. The semiconductor package of Claim 1 wherein:

the first and second surfaces of each of the leads are generally planar and extend in opposed relation to each other;

each of the leads further includes a third surface formed between the first and second surfaces thereof;

the third surface of each of the leads is covered by the encapsulant portion; and

the first surface of each of the leads is exposed within the encapsulant portion to serve as an input/output terminal.

4. The chip package of Claim 1 wherein:

each of the leads includes a bump land formed at

a prescribed region of the second surface thereof; and

the conductive bumps are fused to respective ones of the bump lands of the leads.

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5. The chip package of Claim 4 wherein each of the leads includes a protective layer formed on the second surface thereof other than for the prescribed region including the bump land.

6. The semiconductor package of Claim 5 wherein the protective layer is selected from the group consisting of:

a polyimide;

titanium; and

aluminum.

7. The chip package of Claim 1 wherein:

each of the leads includes:

a pad portion; and

at least one connecting bar portion integrally connected to and extending from the pad portion;

certain ones of the leads each include a bump land formed on the second surface upon the pad portion thereof;

certain ones of the leads each include a bump land formed on the second surface upon the connecting bar portion thereof; and

the conductive bumps are fused to respective ones of the bump lands of the leads.

8. The chip package of Claim 7 wherein:

the pad portions of the leads are segregated into an outer set and an inner set;

the pad portions of the inner set each include a bump land formed thereon; and

at least one connecting bar portion extending from each of the pad portions of the outer set includes a bump land formed thereon.

9. The semiconductor package of Claim 8 wherein:

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the first and second surfaces of each of the leads are generally planar and extend in opposed relation to each other;

each of the leads further includes a third surface formed between the first and second surfaces thereof in opposed relation to that segment of the second surface which extends along the connecting bar portion;

the third surface of each of the leads is covered by the encapsulant portion; and

the first surface of each of the leads extending along the pad portion thereof is exposed within the encapsulant portion to serve as an input/output terminal.